

WHAT IS CLAIMED IS:

1. A static random access memory comprising MOS transistors which each include a channel-forming semiconductor region and a gate electrically connected with each other.

2. A static random access memory as claimed in claim 1, wherein memory cells of the static random access memory each includes:

an N-type MOS transistor having a channel-forming semiconductor region and a gate electrically connected with each other; and

a P-type MOS transistor having a channel-forming semiconductor region electrically connected with a power source.

3. A static random access memory as claimed in claim 2, wherein said P-type MOS transistor has a gate oxide film larger in thickness than said N-type MOS semiconductor transistor.

4. A static random access memory as claimed in claim 2, wherein said channel-forming semiconductor region of the P-type MOS transistor is formed of an N-type well deeper than a P-type well that forms the channel-forming

semiconductor region of the N-type MOS transistor, and these channel-forming semiconductor regions are electrically isolated from each other.

- 5        5.            A static random access memory as claimed in claim 1, comprising write circuit means that include:

         MOS transistors each having a channel-forming semiconductor region and a gate electrically connected with each other.

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6.            A static random access memory as claimed in claim 5, wherein said MOS transistors of the write circuit means include N-type MOS transistors which serve to make a bit line and an inverted bit line have a high-level electric potential, respectively.

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7.            A static random access memory as claimed in claim 1, comprising read circuit means that include MOS transistors each having a channel-forming semiconductor region and a gate electrically connected with each other.

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8.            A static random access memory as claimed in claim 1, wherein memory cells of the static random access memory each include:

an N-type MOS transistor having a channel-forming semiconductor region and a gate electrically connected with each other; and

a resistor.

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9. A semiconductor device, comprising:

first MOS transistors for performing internal processing, which each have a channel-forming semiconductor region formed of a first well; and

10 second MOS transistors for performing direct signal transmission and reception to and from an external device, which each have a channel-forming semiconductor region formed of a second well deeper than the first well.